Tools Tutorial

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Summary:

This document contains some tutorials for the tools used mainly during lecture exercises. They are aimed at getting used to the software environments, gathering tips and tricks, and locating the available resources.

The examples are not analysed in details, and might not be meaningful for real-life usage, but focus on getting a simple task done from A to Z, while covering most of the required functionalities of the software environments.

Last Update: 20.11.2014

1 Analog Design

The analogic circuit design, simulation and layout interface is called "Virtuoso IC". This section will present

For now, the Analogic Design tutorials will be realised using the UMC 65nm design kit, which is the only one installed

1.1 Load the Design Kit

To load the design tools, you just need to load a design kit, which will in Turn load the appropriate software chain. The design kit contains that basic component definitions available in the target technology, like transistors, capacitors etc...

At the command prompt, just source the design kit load script:

\$ source /opt/adl_cadence/umc_65.sh

The source command loads a script as if you had typed the command one by one. If you just run the script by typing /opt/ adl_cadence /umc_65.sh, a process will be created and destroyed at the end of execution, which prevents the modification of the terminal's environment variables, which is necessary for a proper tool loading.

1.2 Work folder preparation

Create a folder dedicated to working with the chosen design kit. Typically, it should be created for a specific project, or set of library components.

For the exercices, one folder is enough:

\$ mkdir das-exercices-umc65 \$ cd das-exercices-umc65

1.3 Start Virtuoso

Just type "virtuoso" at the command prompt:

\$ virtuoso

When starting virtuoso from a location in the file system, it will look for a local "cds.lib" file. This file contains references to other locations on the file system, where some component libraries may be found. It can be edited from Virtuoso by the Library Manager.

By default, the cds.lib file gets populated at least with the location of the design kit technology library provided by the factory, where you can find the base transistor components for example.

The initial GUI is very light, you should only see the console window, which reports various informational and error messages:

	Virtuoso® 6.1.6-64b - Log: /home/rleys/CDS.log	8
Ē	Eile Tools Options Help ca	dence
Lo	bading ci.cxt bading ams.cxt irtuoso Framework License (111) was checked out successfully. Total checkout time was 0.01s.	
 n	nouse L: M:	R:
1	>	

1.4 The Library manager

The various circuits are structured as following:

- ✓ <u>Library</u>: A library contains some Cells
 - o <u>Cells</u>: A Cell represents a circuit, and contain the various views of the cell
 - <u>Views</u>: The views are the various possible descriptions for a cell. For example, a schematic view will be the formal circuit description, while the layout view will be the physical drawing.

The Library Manager in Virtuoso mirrors this organisation. To open it, Click "Tools -> Library Manager":

Library Manager: Directory415/Das	-uebung/exercices-umc65		8
<u>File E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp			cādence
Show Categories Show Files	Cell	View	
analogLib basic cdsDefTechLib umc65II			
Messages Log file is "/ ome/rleys/homes/leys/LS-ADL/WS	31415/DaS-uebung/exercices-umc65/libManage	er.log".	
	100		
cds.lib			

Now we can have a look at the views available for a transistor cell of the design kit library "umc65ll" :

Library Manager: Directory415/DaS-uebung/exe	ercices-umc65	8
<u>Fi</u> le <u>E</u> dit ⊻iew <u>D</u> esign Manager <u>H</u> elp		cādence
Show Categories Show Files Ubrary Umc65ll analogLib	Cell P_25_LL P_12_LLHVT	Symbol View Lock Size
Design Kit Library	P_12_LLHVTRF P_12_LLLVT P_12_LLLVTRF P_12_LLRVT P_12_LLRVTFF P_250033_LL P_25_LLF RM1 RM2 RM3 RM4 RM5 RM6 RM7 RM8	auCdl 19k auLvs 19k hspiceD 19k ivpcell 23k layout 162k symbol 19k
Messages	Transistor cell	
		Symbol Physical Layout
	1001	Lib: umc6511 Free: 482.52G

To edit the view of a cell, just click on the view name and the appropriate editor will start.

1.5 Simple ideal schematic Design

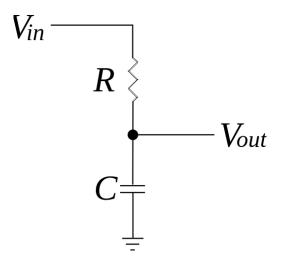
The schematic entry is the first stage of a circuit design. Using the schematic editor, you will:

- ✓ Place, configure and connect the circuit components
- Place, configure and connect simulation components, like voltage sources and signal generators
- ✓ Launch Simulations

The components you can use on you circuit will be available from three main sources:

- ✓ The Technology Library, specific from the target technology.
- ✓ The standard ideal components (Signal sources etc...) from the "analogLib" library.
- ✓ The additional libraries you add to you library manager, which may contain shared and thirdparty components designed for your target technology, or for simulation purpose.

To get used to the Virtuoso environment, we are going to start with a simple RC pass filter circuit, only requiring ideal components:



1.5.1 Cell + Schematic Creation

- ✓ Create a "Tutorial" Library
 - Open The Library Manager, *File -> New -> Library*
 - o Save the Library in the current Folder

New Library	×
Library	
Name Tutorial	
Directory 🔄/WS1415/DaS-uebung/exercices-umc65/ 🔽 (🗢 🗈 💣 🏢 🏢	
, assura_tech.lib cds.lib iibManager.log libManager.log.cdslck umc18-display.drf	
File type: Directories	
Design Manager Use NONE Use No DM Compression enabled	
OK Apply Cancel Help)

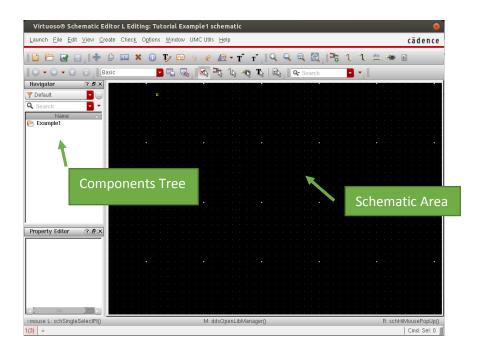
o Attach the library to the design kit technology file

Technology File for New Library 🛛 😵		Attach Library	to Technology Library 🛛 😣
Technology File for library "Tutorial"		New Library	Tutorial
You can: 🔾 Compile an ASCII technology file	N	Technology Library	analogLib
Reference existing technology libraries			basic cdsDefTechLib
 Attach to an existing technology library 			umc6511
Do not need process information			
OK Cancel Help			OK <u>C</u> ancel <u>A</u> pply <u>H</u> elp

✓ Create an "example1" cell, with a schematic view: File -> New Cell View...

New File	8
_ File	
Library	Tutorial 🔽
Cell	example1
View	schematic
Туре	schematic 🔽
Application	
Open with	Schematics L
🔲 Always use ti	his application for this type of file
Library path file	
′WS1415/DaS-ue	bung/exercices-umc65/cds.lib
	OK <u>C</u> ancel <u>H</u> elp

✓ A schematic editor window should open:



Our RC circuit is very simple and only requires ideal components taken from the "analogLib" library, which you can explore from the library manager.

1.5.2 Component instantiation

To add a component to the circuit:

- ✓ Press the I (Instance) key
- ✓ Enter the source library: *analogLib*
- ✓ Enter the component name
- ✓ Select the view type: Symbol
- ✓ (optional) You can add some names for the schematic.

Add	Instance	8
Library	analogLib Browse	
Cell		Component Name
View	symbol	
Names		Instance Name
🗹 Add W	/ire Stubs at: all terminals • registered terminals only	
Array	Rows 1 Columns 1	
	🚯 Rotate 🛛 🕼 Sideways 🛛 🚭 Upside Down	
	Hide <u>C</u> ancel <u>D</u> efaults <u>H</u> el	q

If the selection matches a component, two things happen:

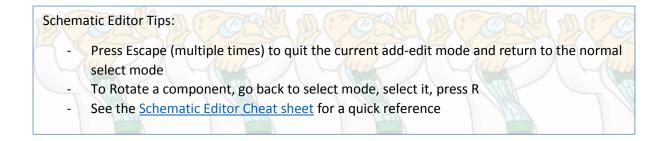
- ✓ The Add Instance window expands to show the component's properties. You can edit them right away or later.
- ✓ You should be able to add the component to the schematic without closing the Add Instance window. Just move the mouse over the schematic area.

For our circuit, we will need:

- ✓ A resistor "res"
- ✓ A capacitor "cap"
- ✓ A Signal generator "vpulse"
- ✓ A Ground component "gnd"

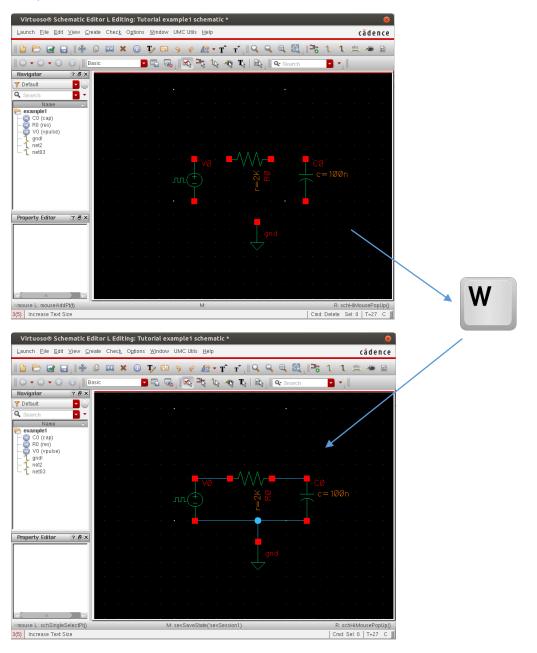
Add those components to the schematic, this is how it looks like for the resistor:

Virtuoso® Schematic Editor L Editing: Tutorial example1 schematic *	8 Add Instance	8
Launch <u>File</u> <u>E</u> dit <u>Vi</u> ew <u>C</u> reate Check Options <u>Wi</u> ndow UMC Utils <u>H</u> elp	cādence	Browse
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Navigator ?	✓ Add Wire Stubs at: ↓ all terminals	• registered terminals only
Y Default Image: Second sec	Array Rows	1 Columns 1
Name	All Rotate (A	Sideways 🛛 🚄 Upside Down
Example1 R0 (res)	Model name	
	Resistance	1K Ohms
	Length	
	Width	
	Muttiplier	
RØ . 🤻 RØ . 🤻	Scale factor	
<r:1K $<$	Temp rise from ambient	
	Temperature coefficient 1	
\sim \cdot	Temperature coefficient 2	
	Resistance Form	
Property Editor 7 6 ×	Generate noise?	
	Capacitance	
	Alias for Lin. temp. co.	
	Alias for Quad temp. co.	
	Lin temp co of lin cap	
	Quad temp co of lin cap	
	Resistance Scaling Factor	
	Capacitance Scaling Factor	
🗶 💷 🚬 🔄 en la construcción de la construcción d	AC resistance	
immouse L: mouseAddPt(t) M: Rotate 90	R: schHiMousePopUp() Temperature difference	
3(5) Point at location for the instance.	Cmd: Instance Sel: 0	<u>Cancel</u> <u>D</u> efaults <u>H</u> elp



1.5.3 Wiring

Once you have added all the components, press the W key to enter wiring mode, and connect the components with each other:



1.5.4 Edit the properties

Now we can edit the properties of the components in our circuit. To do so, select a component, and press Q to access the edit properties window:

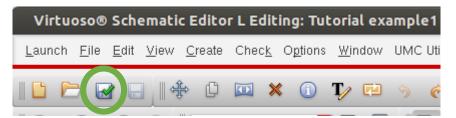
- ✓ Set the vpulse AC parameters:
 - AC Magnitude = 1V
 - \circ AC phase = 0
- ✓ Set the resistor value: 2K
- ✓ Set the capacitor value: 100n

For a simple first-order pass-filter, the cut-off frequency is $=\frac{1}{2\pi RC}$, in our case then around 795Hz. We will try to check this in the simulation.

Apply To	only cu	rrent 🔽 inst	ance 🔽		
Show	🔲 syst	em 🗹 user 🐚	CDF		
	Browse	Reset Ins	tance Labels	Display	
Pro	perty		Value		_
Libra	ary Name	analogLib			0
Cell	Name	vpulse			0
Viev	v Name	symbol			0
Insta	ince Name	V0			0
		Add	Delete	Modify)
Use	er Property	Master 1	√alue	Local Value	
Ivs	Ignore	TRUE			0
CD	F Parameter		Value		
Frequency n	ame for 1/pei	riod			0
Noise file nar	ne				0
Number of no	ise/freq pairs	0			0
DC voltage					0
AC magnitud	е	1 V			o
AC phase		0			o
XF magnitude	9				o
PAC magnitu	de				0
PAC phase					0
Voltage 1					0
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1.5.5 Check and save the circuit

After any change to the circuit, click on the check and save button to verify the circuit's basic connectivity, and generate the correct netlist. If an error occurs, a message window will pop-up, and a log output will be written to the console window.



1.5.6 Run a simulation

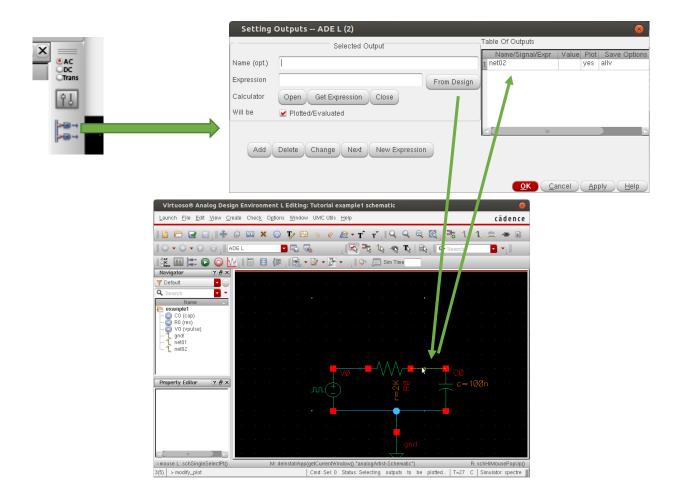
ADE L (2) - Tutorial example1 sc	hematic	8	
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Design Variables	Analyses Type Enable Argun	? B ×	Analyses Selection
Name Value		Rule Save Options	Plot Output Selection
22(43) Setup Outputs	Status: Ready	T=27 C Simulator: spectre	

Now we are ready to run a Simulation. Click on Launch -> ADE L to open the simulation environment:

Let's setup the simulation:

- ✓ First select an analysis type by clicking the Analyses selection button:
 - The Analysis window allows configuring all the enabled analysis.
 - We want to perform a Frequency response analysis.
 - Select the "ac" anaylis
 - Set Sweep Variable to Frequency
 - Set the Start and Stop values of the sweep range to 1 1G (1hz to 1Ghz)
- ✓ Then, select to output to be plotted by clicking the output selection button:
 - You can select the output by entering node names per hand
 - Otherwise, click on the "From Design" button, and click on the schematic to add a node or wire to the outputs.
 - When finished adding the outputs, press Esc on the schematic and close the dialog box.
 - \circ $\;$ Add the Wire between the resistor and capacitor as output:

Choosing	g Analyses	ADE	L (2)		8
Analysis	🔾 tran	🔾 dc	🖲 ac	🔾 noise	
	🔾 xf	🔾 sens	🔾 dcmatch	🔾 stb	
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss	
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac	
	🔾 hbnoise	🔾 hbsp			
		AC Ana	dysis		
Sweep Var	iable				
Freque	ncy				
Design	Variable				
🔾 Temper	ature				
Comport	nent Paramet	er			
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None					
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 Start-St 	^{op} s	tart 1	s	itop 16	
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	_				
Add Specific	e Points 📃				
Specialized	d Analyses				
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	<u>0</u> K	<u>C</u> ancel	Defaults	Apply H	elp



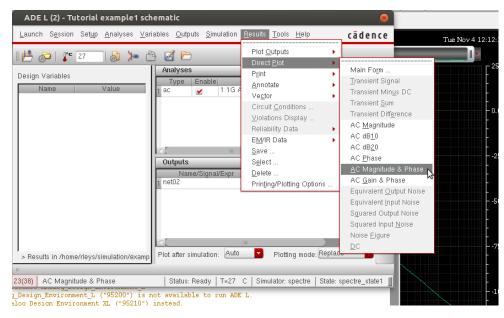
Now the simulation window is ready, we can run the simulation by clicking the play button:

ADE L (2) - Tutorial example1 sch	ematic	8
Launch S <u>e</u> ssion Set <u>u</u> p <u>A</u> nalyses <u>V</u> aria	ables <u>O</u> utputs <u>Si</u> mulation <u>R</u> esults <u>T</u> ools <u>H</u> elp	cādence
I 🛃 🔊 🦵 27 🛛 👵 🎾 🖆) 🗹 🗁	
Design Variables Name Value	Analyses Type Enable Arguments 1 ac ⊻ 1 1G Automatic Start-Stop	?
	Outputs Name/Signal/Expr Value 1 net02 Image: Constraint of the second	? ₽ ¥ ¥ Options
> Results in /home/rleys/simulation/examp	Plot after simulation: Auto Plotting mode: Replace	ator: spectre

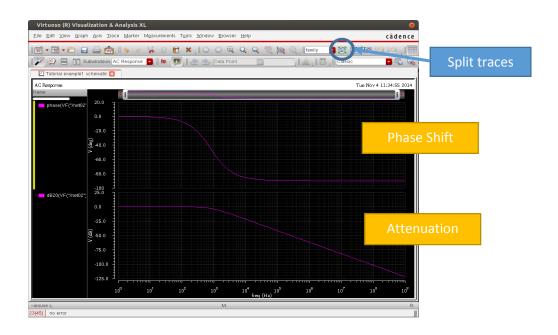
The output plot should appear automatically, and show the output voltage based on the frequency. However, for that kind of analysis, we want to see the Bode Plot showing the attenuation and phase shift, so that we can check our cut-off frequency.

To do so, go back to the main simulation window:

- ✓ Select Results -> Direct Plot -> AC Magnitude an Phase
- ✓ The schematic window will come in front



- ✓ Select the output wire, as for the output selection
- ✓ Press Esc
- ✓ The Plot window should come back with the Magnitude in db and Phase shift traces.
- ✓ You can use the split traces button to display the traces separately



The cut-off frequency is defined for an attenuation of 3db (half of the input). You can use the mouse to search for the point.

1.5.7 Save and restore simulation state

Now that we have performed our simulation, we can save its configuration (aka state) and reload it later. To do so, go back to the simulation window:

- ✓ To save, click on Session -> Save State...
 - On the dialog, set Save State Option: CellView (the state will be saved as a view of the cell)
 - Under CellView Options, you can change the name of the state
 - You can use a different save mode if you like, but this one is quite convenient.
- ✓ To restore, click on Session -> Load State...
 - \circ $\;$ The dialog box the same as the save one, just set the same values.

Save State Option	🔾 Directory 🖲 Cellv	iew
Directory Options		
State Save Directory	~/.artist_states	Browse.
Save As	state1	
Existing States		
Cellview Options	Tutorial	
Library		
Cell	example1 Br	owse
State	spectre_state1	
Description		
Description None	ш	
	ш	2
None		Select All Clear All
None	™ ✓ Variables	Select All Clear All
None What to Save ✓ Analyses ✓ Subckts	⊻ Variables ⊻ Model Setup	 ✓ Outputs ✓ Simulation Files
None What to Save ✓ Analyses ✓ Subckts ✓ Environment Opt	✓ Variables ✓ Model Setup ions ✓ Simulator Options	 ✓ Outputs ✓ Simulation Files ✓ Convergence Setup
None What to Save ✓ Analyses ✓ Subckts ✓ Environment Opt ✓ Waveform Setup	⊻ Variables ⊻ Model Setup ions ⊻ Simulator Options ⊻ Graphical Stimuli	 ✓ Outputs ✓ Simulation Files ✓ Convergence Setup ✓ Conditions Setup
None What to Save ✓ Analyses ✓ Subckts ✓ Environment Opt ✓ Waveform Setup	 ✓ Variables ✓ Model Setup ions ✓ Simulator Options ✓ Graphical Stimuli Setup ✓ Device Checking Setup 	 ✓ Outputs ✓ Simulation Files ✓ Convergence Setup ✓ Conditions Setup

1.6 Complete Physical Circuit with Layout Editor

Now that we have completed a simple simulation for an ideal circuit, we are going to see how to implement a CMOS inverter UMC65nm.

Questions:

- ✓ Schematic:
 - \circ Why do we need pins for bulk contact, (not directly connected)
 - AW: Keep the option to connect to different voltage source
 - Simulation:
 - Simulate on same schematic?
 - create a new view with the symbol?
- ✓ Symbol:
 - Import definitions from schematic -> Schematic -> Edit -> create Cellview from cellview
 - o Edit -> Origin
 - \circ Selection box
 - o Move around stuff
- ✓ Testbench
 - o Create Labels

1.6.1 Schematic

- 1.6.2 Symbol
- 1.6.3 Testbench

1.6.4 Physical Layout

- ✓ Pins not necessary
- ✓ Wires connect to correct anme
- ✓ Add vias for input
 - Maybe not depending on usage
- ✓ Add via for nwell-psub

1.6.5 DRC

1.6.6 LVS

1.7 Virtuoso Cheat Sheet

1.7.1 Schematic Editor

Keyboard	Command	Description		
All modes				
Esc	Quit mode (Back to select)			
Select Mode				
I	Add a component			
W	Enter wiring mode			
L	Add a Name Label			
Μ	Move an object	First Click the object to move, then drag. Direct dragging will usually drag the previously selected object.		
Ρ	Add a Pin			
F	Fit	Zoom to fit the whole schematic in the window		
Delete	Enter Delete Mode	Click anything to delete it		
Selected Mode				
Q	Edit Properties			
R	Rotate			

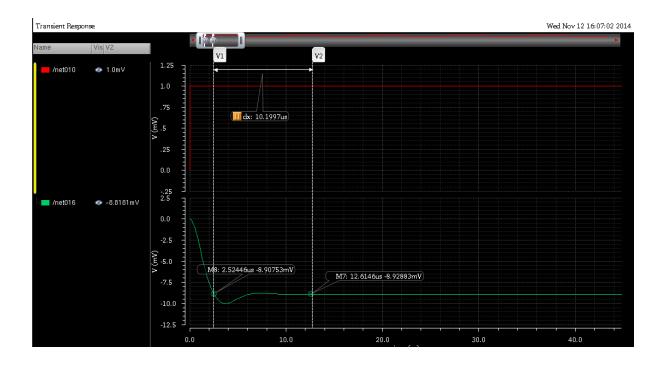
1.7.2 Simulation Browser (ADE)

Keyboard	Command	Description
Μ	Add a Marker on the curve	Move the along the curve, and press M to place a marker at mouse position
V	Add a vertical marker on the graph	Move the along the curve, and press V to place a marker at mouse position

1.7.2.1 Delta Marker

To create a delta (difference) marker between two vertical markers:

- ✓ Place your vertical markers
- \checkmark Select them with clicking them while holding control
- ✓ Press Shift + D



1.7.3 Layout Editor

Keyboard	Command	Description			
All modes					
Esc	Quit mode (Back to select)				
Select Mode	Select Mode				
	Add a component				
L	Label Shape				
Μ	Move an object	First Click the object to move, then drag. Direct dragging will usually drag the previously selected object.			
0	Create a Via				
Ρ	Wire Shape				
R	Rectangle Shape				
S	Shape/Reshape	Got to select mode, activate reshape mode, then click on the side handles of the object to reshape once, and move the mouse to reshape (don't drag the mouse)			
F	Fit	Zoom to fit the whole schematic in the window			
Delete	Enter Delete Mode	Click anything to delete it			
Selected Mode					
R	Rotate				
Q	Edit Properties				